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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,120	09/22/2003	Takashi Miyazawa	117244	5416

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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,120	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *9-12,and 15-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,14 and 20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-5** are rejected under 35 U.S.C. 102(b) as being anticipated by Dawson et al. (Patent No.: US 6,229,506 B1).

With respect to **Claim 1**, Dawson teaches an electronic circuit *(See figure 2)*, comprising: a capacitor *(element 280; column 3, lines 50-52)* that is capable of accumulating a current signal and a voltage signal in a form of an amount of charge *(note that a current signal is supplied to the capacitor by the data line, element 220, note that the capacitance of a capacitor is the difference of charges across the capacitor plates giving rise to a voltage, thus the capacitor is capable of accumulating a current signal and a voltage signal in a form of an amount of charge)*; and a first transistor *(element 260; column 3, line 64 to column 4, line 5; column 3, lines 36-39)* whose conduction state is set in accordance with the amount of charge accumulated in the capacitor, the first transistor including a first gate, a first drain and a first source, the first transistor supplying a current whose amount is determined in accordance with the conduction state to an electronic element.

With respect to **Claim 2**, the electronic circuit according to Claim 1, Dawson teaches a second transistor *(See figure 2, element 250)*, the current signal and the voltage signal being supplied to the capacitor through the second transistor *(column 3, lines 15-16; note the above discussion of current and voltage on the capacitor)*.

With respect to **Claim 3**, the electronic circuit according to Claim 1, Dawson teaches a third transistor *(See figure 2, element 240)* that controls an electronic connection between the first gate and the first drain *(column 3, lines 18-20)*.

With respect to **Claim 4**, the electronic circuit according to Claim 1, Dawson teaches a fourth transistor *(See figure 2, element 250; column 3, lines 36-39 and lines 55-57)* that controls a timing to start or stop supply of the current to the electronic element after the conduction state of the first transistor *(element 260)* is set according to at least one of the current signal and the voltage signal.

With respect to **Claim 5**, the electronic circuit according to Claim 1, Dawson teaches a fifth transistor *(element 270; column 3, lines 20-22 and lines 44-52)*, the amount of charge held in the capacitor being reset to a predetermined state when the fifth transistor is turned on.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 6-8, 13-14, 20, 22-26 and 28-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson in view of Tsuchida et al. (Pub. No.: US 2002/0196215 A1).

With respect to **Claim 6**, Dawson teaches an electro-optical device *(See figure 1)*, comprising: a plurality of scanning lines *(130a, 130b, ...)*, a plurality of data lines *(140a, 140b, ...)*, and a plurality of unit circuits *(See figure 2)*. Dawson does not teach the electro-optical device comprising a first circuit that outputs a current signal that is accumulated in a capacitor included in each of the plurality of unit circuits, nor does Dawson teach a second circuit that outputs a voltage signal that is accumulated in a capacitor in each of the plurality of unit circuits.

Tsuchida teaches a data line driving circuit *(See figure 1, element 2)* that comprises a first circuit *(CB1, CB2, ..., CB256)* that outputs a current signal and a second circuit *(V1, V2, ..., V256)* that outputs a voltage signal *([0029], lines 1-3)*. Tsuchida teaches the use of driving switches *(D1, D2, ..., D256)* for selection of the either the constant voltage source or constant current source *([0029], lines 1-3)*.

The electro-optical device of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data line driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in a current signal that is accumulated in a capacitor included in each of the plurality of unit circuits; and a voltage signal that is

accumulated in a capacitor in each of the plurality of unit circuits through the use of driving switches for selection of the source.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electro-optical device of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **<u>Claim 23</u>**, Dawson teaches an electronic circuit *(See figure 2)*, comprising: a capacitor *(element 280; column 3, lines 50-52)* that accumulates a current signal and a voltage signal *(note that a current signal is supplied to the capacitor by the data line, element 220, note that the capacitance of a capacitor is the difference of charges across the capacitor plates giving rise to a voltage, thus the capacitor is capable of accumulating a current signal and a voltage signal in a form of an amount of charge)*, a first transistor *(element 260; column 3, line 64 to column 4, line 5; column 3, lines 36-39)* whose conduction state is set in accordance with an amount of charge accumulated in the capacitor, and the first transistor including a first gate, a first drain and a first source, the first transistor supplying a current whose amount is determined in accordance with the conduction state to an electronic element. Dawson does not teach an electronic circuit comprising a capacitor that accumulates a current signal during a first period and nor does Dawson teach the capacitor accumulating a voltage signal during a second period.

Tsuchida teaches a data line driving circuit *(See figure 1, element 2)* that comprises a first circuit *(CB1, CB2, ..., CB256)* that outputs a current signal and a second circuit *(V1, V2, ..., V256)* that outputs a voltage signal *([0029], lines 1-3)*. Tsuchida teaches the use of driving switches *(D1, D2, ..., D256)* for selection of the either the constant voltage source or constant current source *([0029], lines 1-3)*.

The electro-optical device of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data line driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in a capacitor that accumulates a current signal during a first period and the capacitor accumulating a voltage signal during a second period through the use of driving switches for selection of the source. The first period being the time when the switches connect the data line to the current sources and the second period being the time when the switches connect the data line to the voltage sources.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electro-optical device of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 24**, Dawson teaches an electronic circuit *(See figure 2)*, comprising: a capacitor *(element 280; column 3, lines 50-52)* that accumulates a current signal and a voltage signal *(note that a current signal is supplied to the capacitor by the data line, element 220, note that the capacitance of a capacitor is the difference of charges across the*

capacitor plates giving rise to a voltage, thus the capacitor is capable of accumulating a current signal and a voltage signal in a form of an amount of charge), a first transistor *(element 260; column 3, line 64 to column 4, line 5; column 3, lines 36-39)* whose conduction state is set in accordance with an amount of charge accumulated in the capacitor, and the first transistor including a first gate, a first drain and a first source, the first transistor supplying a current whose amount is determined in accordance with the conduction state to an electronic element. Dawson does not teach an electronic circuit comprising a capacitor that accumulates a current signal during a first mode and nor does Dawson teach the capacitor accumulating a voltage signal during a second mode.

Tsuchida teaches a data line driving circuit *(See figure 1, element 2)* that comprises a first circuit *(CB1, CB2, ..., CB256)* that outputs a current signal and a second circuit *(V1, V2, ..., V256)* that outputs a voltage signal *([0029], lines 1-3)*. Tsuchida teaches the use of driving switches *(D1, D2, ..., D256)* for selection of the either the constant voltage source or constant current source *([0029], lines 1-3)*.

The electro-optical device of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data line driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in a capacitor that accumulates a current signal during a first mode and the capacitor accumulating a voltage signal during a second mode through the use of driving switches for selection of the source. The first mode is equivalent to the switches connecting the data line to the current sources and the second mode is equivalent to the switches connecting the data line to the voltage sources.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electro-optical device of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

With respect to **Claim 7**, the electro-optical device according to Claim 6, the modified circuit of Dawson by Tsuchida teaches the current signal and the voltage signal being supplied to each of the plurality of unit circuits through one data line of the plurality of data lines *(Tsuchida: See figure 1, A1, A2, ..., A256: data lines)*.

With respect to **Claim 8**, the electro-optical device according to Claim 6, the modified circuit of Dawson by Tsuchida teaches the plurality of data lines *(Tsuchida: See figure 1, A1, A2, ..., A256: data lines)* including a plurality of first data lines and a plurality of second data lines, the current signal being supplied to each of the plurality of unit circuits through one first data line of the plurality of first data lines *(Tsuchida: See figure 1, elements CB1, CB2, ..., CB256; note that the first data lines are equivalent to the data lines when the switches, D1, D2, ..., D256 are connected to elements CB1, CB2, ..., CB256)*; and the voltage signal being supplied to each of the plurality of unit circuits though one second data line of the plurality of second data lines *(Tsuchida: See figure 1, elements V1, V2, ..., V256; note that the second data lines are equivalent to the data lines when the switches, D1, D2, ..., D256 are connected to elements V1, V2, ..., V256)*.

With respect to **Claim 13**, the electro-optical device according to Claim 22, Dawson teaches the electro-optical element being an EL element *(See figure 2, element 290: OLED)*.

With respect to **Claim 14**, the electro-optical device according to Claim 13, Dawson teaches the EL element including a light-emitting layer that is composed of an organic material *(See figure 2, element 290: OLED; column 2, lines 60-66)*.

With respect to **Claim 20**, Dawson teaches an electronic apparatus comprising an electro-optical device *(See figures 1 and 2, element 290: OLED)* according to Claim 6.

With respect to **Claim 22**, an electro-optical device according to Claim 6, Dawson teaches each of the plurality of unit circuits including an electro-optical element *(See figure 2, element 290: OLED)*.

With respect to **Claims 25 and 26**, the electronic circuit according to Claims 23 and 24 respectively, the modified circuit of Dawson by Tsuchida teaches the current signal corresponding to analog data *(Tsuchida: See figure 1, CB1, CB2, ..., CB256; note that a constant current supplies a constant current irrespective of the load across is terminals, thus the voltage is variable and the current signal corresponds to analog data)*, and the voltage signal corresponding to digital data *(note that the voltage signal of Tsuchida is a binary data voltage because binary data is either 0 or 1, which is equivalent to 0V or a certain voltage level)*.

With respect to **Claim 28**, the electronic circuit according to Claim 23, Dawson teaches a second transistor *(See figure 2, element 250)*, the current signal and the voltage signal being supplied to the capacitor through the second transistor *(column 3, lines 15-16; note the above discussion of current and voltage on the capacitor)*.

With respect to **Claim 29**, the electronic circuit according to Claim 23, Dawson teaches a third transistor *(See figure 2, element 240)* that controls an electrical connection between the first gate and the first drain *(column 3, lines 18-20)*.

3. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson, as applied to Claim 1 above, in view of Tsuchida and further in view of Adachi et al. (Pub. No.: US 2003/0058195 A1).

With respect to **Claim 21**, the electronic circuit according to Claim 1, Dawson does not teach the current signal being a multi-valued data current, and does not teach the voltage signal being a binary data voltage.

Tsuchida teaches a data line driving circuit *(See figure 1, element 2)* that comprises constant current sources *(CB1, CB2, ..., CB256)* that outputs a current signal and constant voltage sources *(V1, V2, ..., V256)* that outputs a voltage signal *([0029], lines 1-3)*. Tsuchida teaches the use of driving switches *(D1, D2, ..., D256)* for selection of the either the constant voltage source or constant current source *([0029], lines 1-3)*. The voltage signal of Tsuchida is a

binary data voltage because binary data is either 0 or 1, which is equivalent to 0V or a certain voltage level.

The electro-optical device of Dawson is modified by Tsuchida in such a way that the data line *(See figure 2, element 220)* of Dawson is replaced by the data line driving circuit *(See figure 1, element 2)* of Tsuchida so that the modification results in a current signal that is accumulated in a capacitor included in each of the plurality of unit circuits; and a voltage signal being a binary voltage signal is accumulated in a capacitor in each of the plurality of unit circuits through the use of driving switches for selection of the source.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the data line of Tsuchida to the electro-optical device of Dawson so as to provide a display that requires a shorter time to emit light with a desired instantaneous brightness and has less variation in instantaneous brightness during a scanning period *(Tsuchida: [0010])*.

Tsuchida does not teach the current signal being a multi-valued data current.

Adachi teaches a data current being a multi-value data current *([0033], lines 2-8; [0097])*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data current being a multi-value data current, as taught by Adachi, to the electronic circuit of Dawson as modified by Tsuchida, so as to be able to increase the number of display gray scale without increasing the number of subframes *([0033], lines 6-8)* and to prevent image quality degradation such as dynamic contouring without increasing power *([0104])*.

4. **Claim 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson in view of Tsuchida as applied to claims 23 and 24 above, and further in view of Senda et al. (Pub. No.: US 2002/0171607 A1).

With respect to **Claim 27**, the electronic circuit according to Claim 24, neither Dawson nor Tsuchida mention a power consumption in the second mode being lower than a power consumption in the first mode.

Senda teaches switching between an analog image signal display, which is a first mode and a digital image signal display, which is a second mode. Senda teaches the second mode is lower in power consumption than in the first mode *([0019], lines 1-6)*.

It would have been obvious for a person of ordinary skill in the art to have a power consumption in the second mode being lower than a power consumption in the first mode, as taught by Senda to the electronic circuit of Dawson as modified by Tsuchida, so a to provide a device with power saving capabilities *(Senda: [0075])*.

Response to Arguments

5. Applicant's arguments filed 8/15/2006 have been fully considered but they are not persuasive.

Applicant argues that the combination of Dawson and Tsuchida would not have achieved the capacitor recited in claims 1 and 6 of the amended claims dated 12/18/2003, because neither

of the constant voltage sources nor the constant current sources determine the conduction state of the transistor.

The examiner disagrees. The claim limitation does not recite the current sources or the voltage sources determine the conduction state of the transistor. As the reference Dawson states, "… a pixel structure can be loaded with data by activating the proper select line. Namely, when the select line is set to "Low", transistor P4 is turned "On", where the voltage on the side of the OLED is transmitted to the gate of the transistor P2." *(column 3, lines 32-34)*. Thus, the combined references of Dawson and Tsuchida is valid because the conduction state of the transistor P2 by the current source or voltage source is determined by the select line in combination with transistors P1 and P4.

6. Applicant's arguments with respect to claims 1-8, 13-14 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
SUPERVISORY PATENT EXAMINER
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